



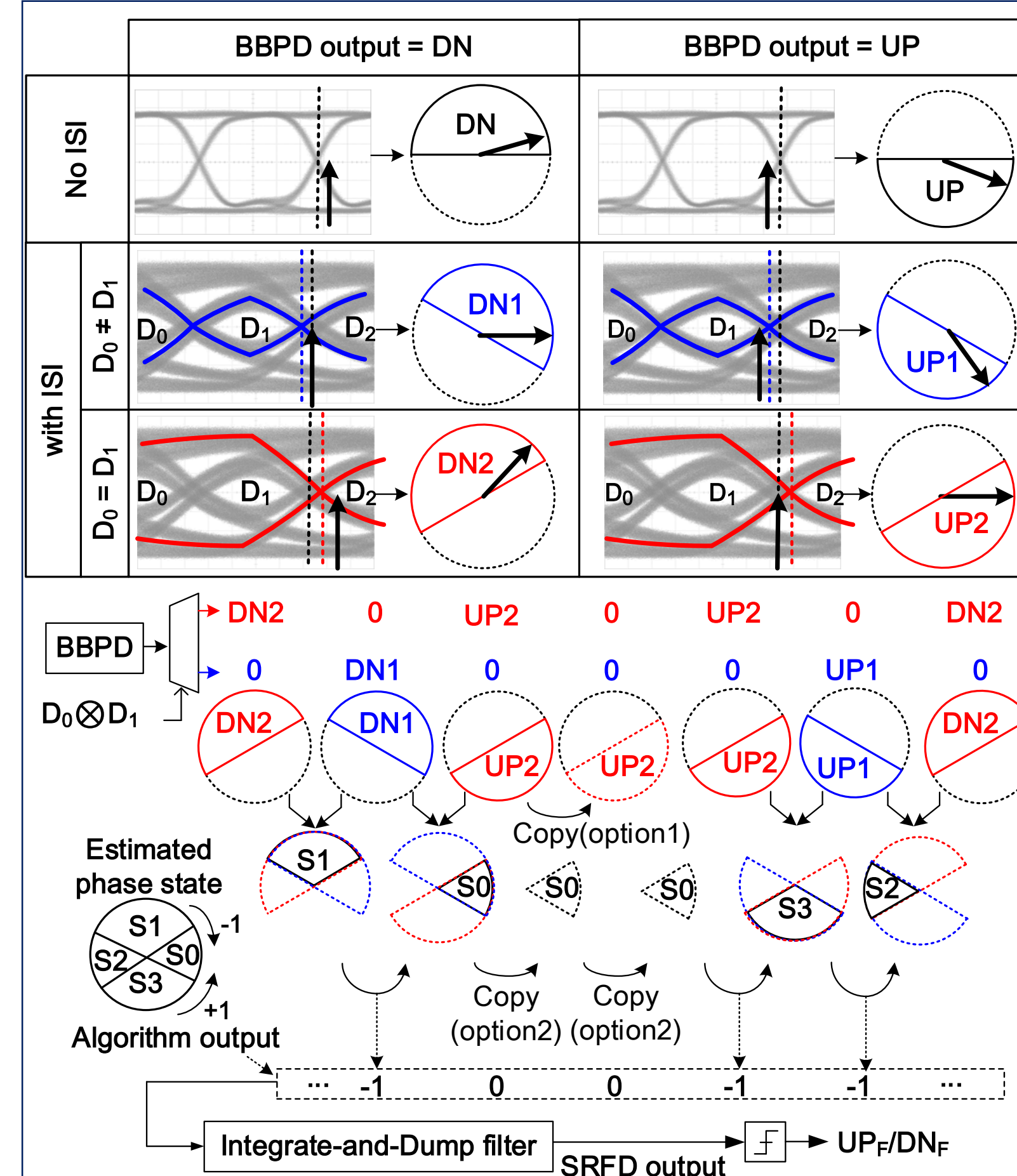
A fully-digital semi-rotational frequency detection algorithm for bang-bang CDRs

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Background

This work presents a new frequency acquisition method using semi-rotational frequency detection (SRFD) algorithm for a reference-less clock and data recovery (CDR) in a serial-link receiver. The proposed SRFD algorithm classifies the bang-bang phase detector(BBPD) outputs to estimate the current phase state, and detects the frequency mismatch between the input data and the sampling clock. The VCO-track path in a digital loop filter (DLF) enables online calibration of a drifted frequency of VCO caused by temperature or voltage variation after a frequency acquisition. The proposed algorithm can be implemented as a digitally-synthesized circuit, lowering design efforts for reference-less CDRs. A 10 Gbps transceiver IC with the proposed algorithm, fabricated in a 65nm CMOS process, demonstrates successful recovery of the input phase without any reference clock.

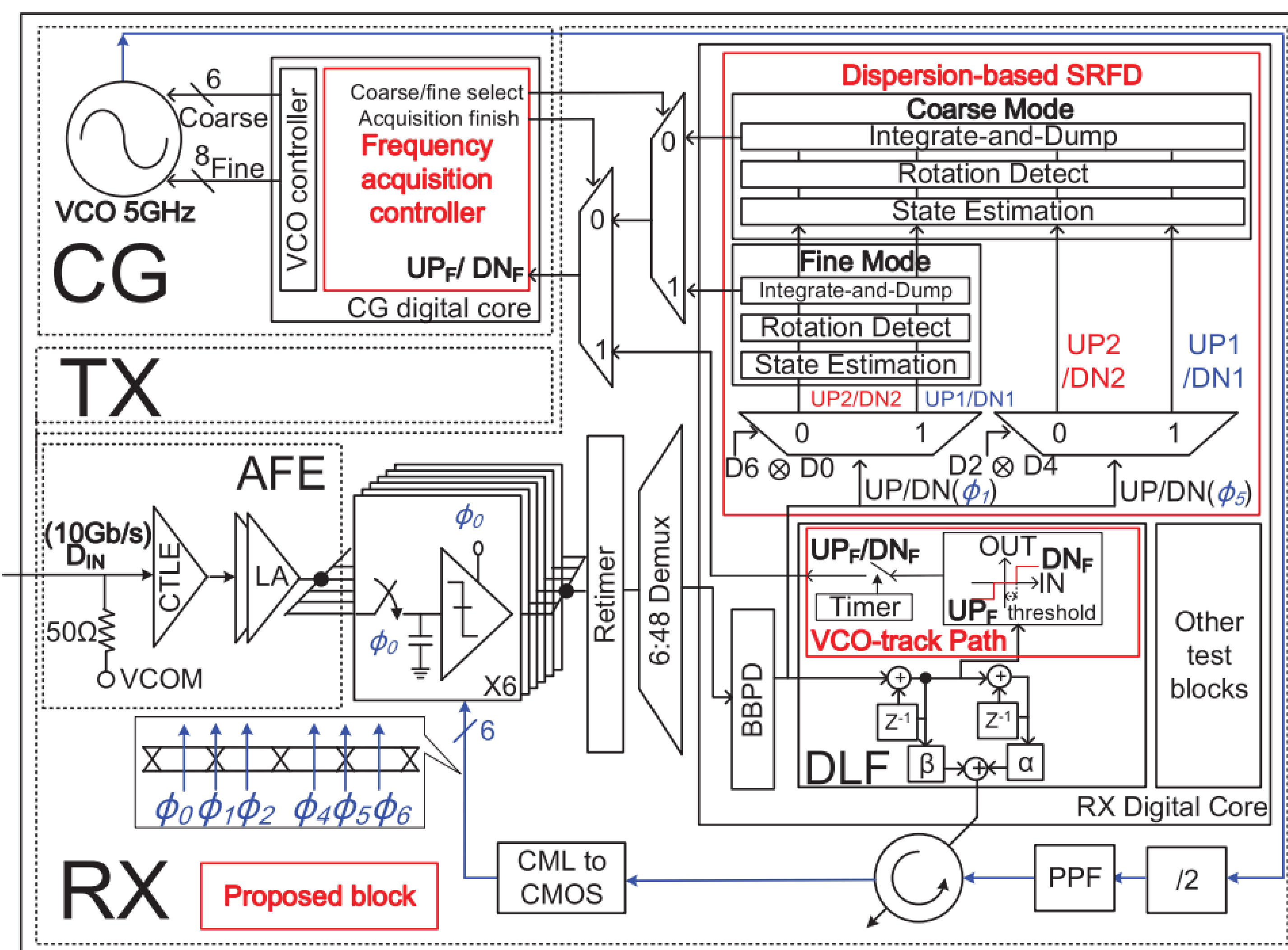
Basic concept of SRFD



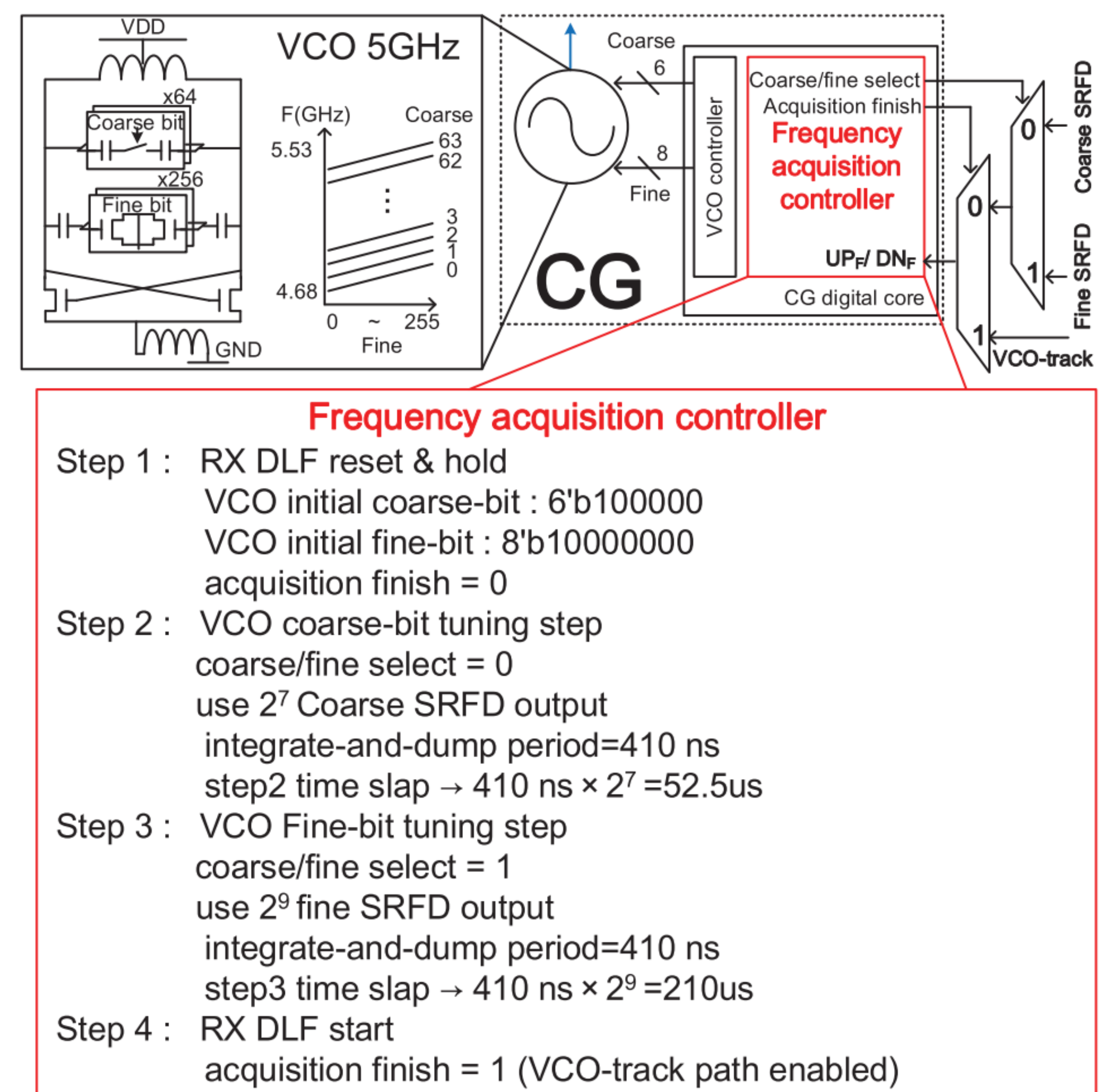
- Exploit ISI to extract frequency information
- Fully synthesized digital algorithm
- 4 different types of SRFD are available by combining option1 and option2.
- frequency detection from 2⁷ PRBS pattern is possible by turning off option2.

Overall Transceiver Architecture

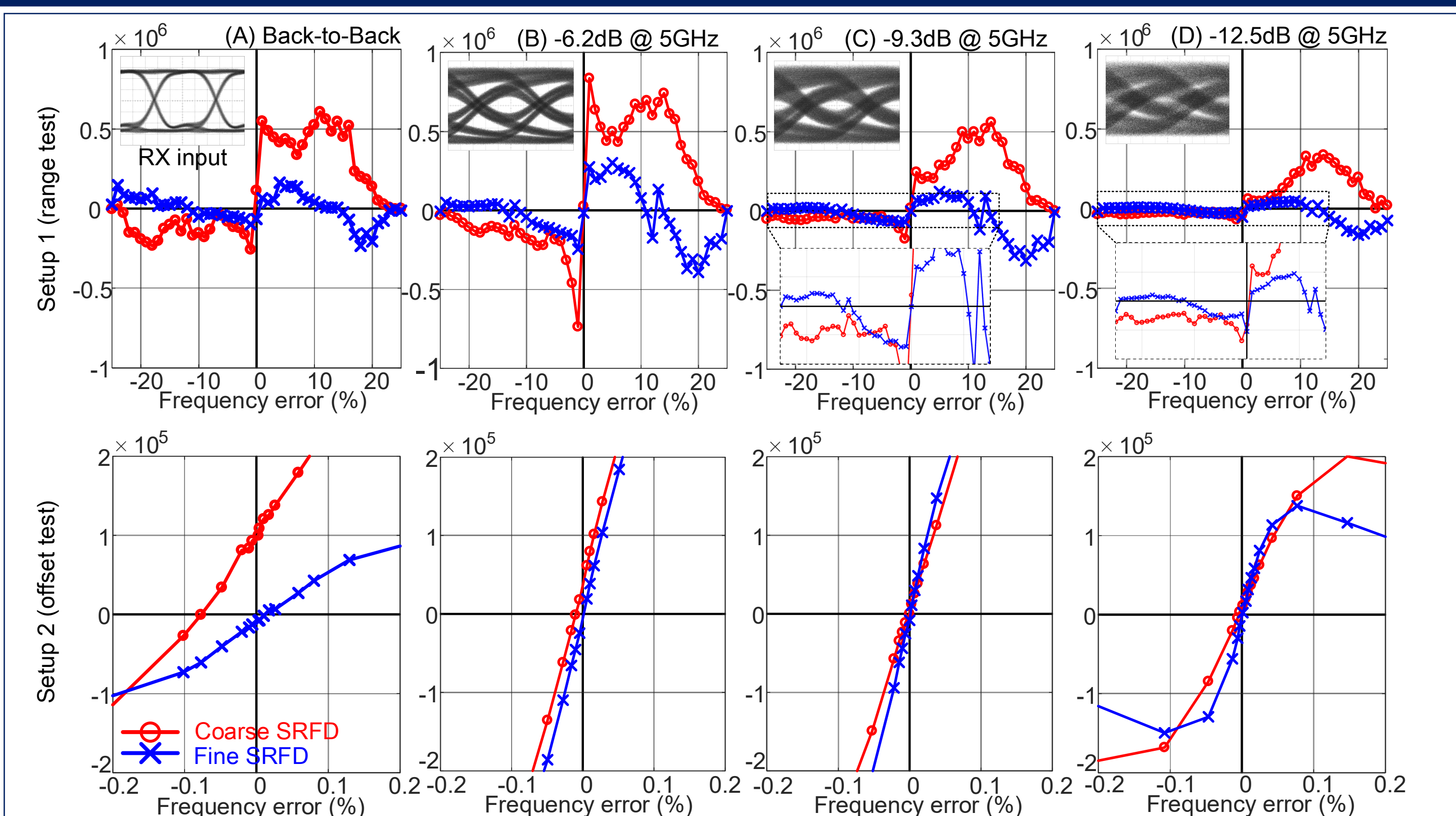
Top Architecture



Frequency acquisition sequence



measured SRFD output



chip photo

